1. A method of generating a logic design for use in designing an integrated circuit (IC), comprising:

embedding a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design.

2. The method of claim 1, further comprising generating the combinatorial one-dimensional logic block.

3. The method of claim 2, further comprising importing the combinatorial one-dimensional logic block.

4. The method of claim 3, further comprising following a set of design capture rules.

5. The method of claim 4, further comprising notifying a designer when capturing data violates the set of design capture rules.

6. The method of claim 1, further comprising using a set of abstractions.

7. The method of claim 1, further comprising generating C++ from the unified database.

8. The method of claim 7, further comprising generating Verilog from the unified database

9. The method of claim 1, wherein the two-dimensional schematic presentation includes a set of Register Transfer Diagrams (RTD).

10. The method of claim 1, further comprising generating synthesizable Verilog from the unified database.

11. An article comprising a machine-readable medium which stores executable instructions to generate a logic design for use in designing an integrated circuit (IC), the instructions causing a machine to:

embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design.

12. The article of claim 11, further comprising instructions to generate the combinatorial one-dimensional logic block.

13. The article of claim 12, further comprising instructions to follow a set of design capture rules.

14. The article of claim 13, further comprising instructions to import the combinatorial one-dimensional logic block.

15. The article of claim 14, further comprising instructions to notify a designer when capturing data violates the set of design capture rules.

16. The article of claim 11, further comprising to use a set of abstractions.

17. The article of claim 11, further comprising instructions to generate C++ from the unified database.

18. The article of claim 12, further comprising instructions to generate Verilog from the unified database.

19. The article of claim 11, wherein the two-dimensional schematic presentation includes a set of Register Transfer Diagrams (RTD) having a set of library elements.

20. The article of claim 11, further comprising instructions to generate synthesizable Verilog from the unified database.

21. An apparatus for generating a logic design for use in designing an integrated circuit (IC), comprising:

a memory that stores executable instructions; and

a processor that executes the instructions to:

embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design.

22. The apparatus of claim 21, further comprising instructions to generate the combinatorial one-dimensional logic block.

23. The apparatus of claim 22, further comprising instructions to follow a set of design capture rules.

24. The apparatus of claim 23, further comprising instructions to import the combinatorial one-dimensional logic block.

25. The apparatus of claim 24, further comprising instructions to notify a designer when capturing data violates the set of design capture rules.

26. The apparatus of claim 21, further comprising instructions to use a set of abstractions.

27. The apparatus of claim 21, further comprising instructions to generate C++ from the unified database.

28. The apparatus of claim 27, further comprising instructions to generate Verilog from the unified database

29. The apparatus of claim 21, wherein the two-dimensional schematic presentation includes a set of register transfer diagrams (RTD) having a set of library elements.

30. The apparatus of claim 29, further comprising instructions to generate synthesizable Verilog from the unified database.